Reducing the Substrate Losses of RF Integrated Inductors

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***Abstract*—This letter introduces a new method for reducing the substrate-related losses of integrated spiral inductors for radio frequency (RF) applications. Measurement based equivalent circuit parameters are demonstrated. Using our method the quality factor increased from 5.3 to 6.0 at 3.5 GHz at an 1.8-nH inductor.**

***Index Terms*—Integrated inductor, on-chip spiral, quality factor, substrate loss.**

I. Introduction

AT SILICON radio frequency (RF) integrated circuits, the usage of on-chip inductors in *LC* tanks is limited by the achievable quality factor. The modeling of such structures was carefully investigated [1], [2], and the source of losses were described as well [3], [4]. To find the optimal geometry, several "guidelines" were defined [2], [3] and optimizing algorithms were established in computer programs [5]. We can find the optimal line width for the highest possible quality factor for a given size and inductance value at a given frequency, but there have not been any suggestions published yet on how to reduce the substrate-related losses.

II. Reducing the Substrate Losses

By optimizing the spiral geometry, we will end up with a line width which will move the maximum of the $Q(f)$ curve to the desired frequency. In this case, the ohmic losses and the substrate capacitance will give us the minimal effective resistivity R_{eff} (where $Z_{\text{in}} = R_{\text{eff}} + j\ \omega^* L_{\text{eff}}$). The substrate used to be considered a limiting factor that we could not change, or that we had to remove [6].

Since the substrate losses at the silicon substrates are related to its semiconductor nature we cannot easily reduce them. The losses are caused by the eddy currents induced by the magnetic filed of the spirals. The eddy currents are flowing around the axis of the spiral. If we can reduce the eddy currents, the quality factor of the spirals will increase. With our BiCMOS technology, most of the substrate currents flow in the top heavily doped p+ layer. This layer can be broken by n+ regions. If we insert n+ regions (narrow stripes) perpendicular to the eddy-current flow we create a blocking p-n-p junction against these currents. The layout of the spiral with the eddy-current blocking structure is shown on Fig. 1.

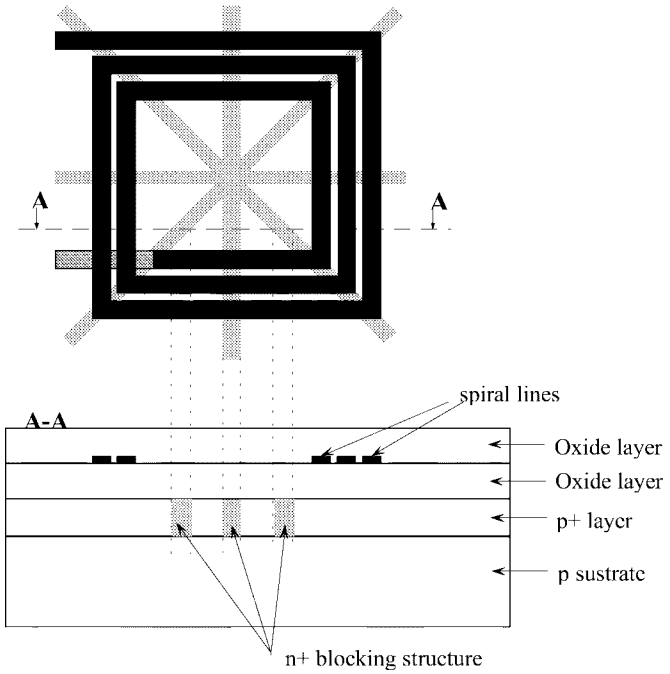

Fig. 1. Integrated spiral with eddy-current blocking structure.

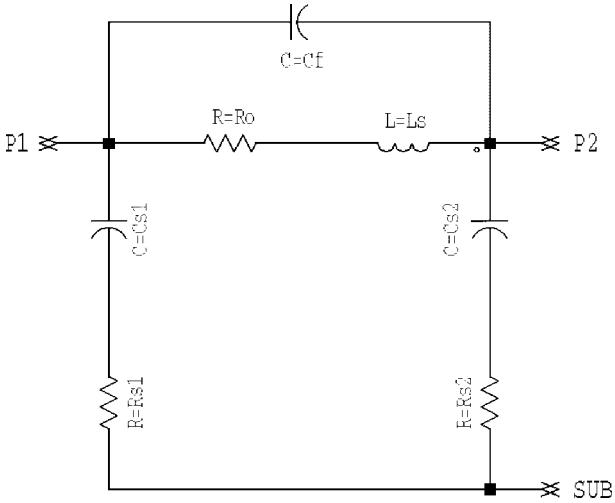

Fig. 2. The compact model of an integrated spiral.

III. Measurement Results

To verify our idea we manufactured identical spirals with and without the blocking structure. We carried out S-parameter

Manuscript received April 20, 1998.

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Publisher Item Identifier S 1051-8207(98)07952-5.

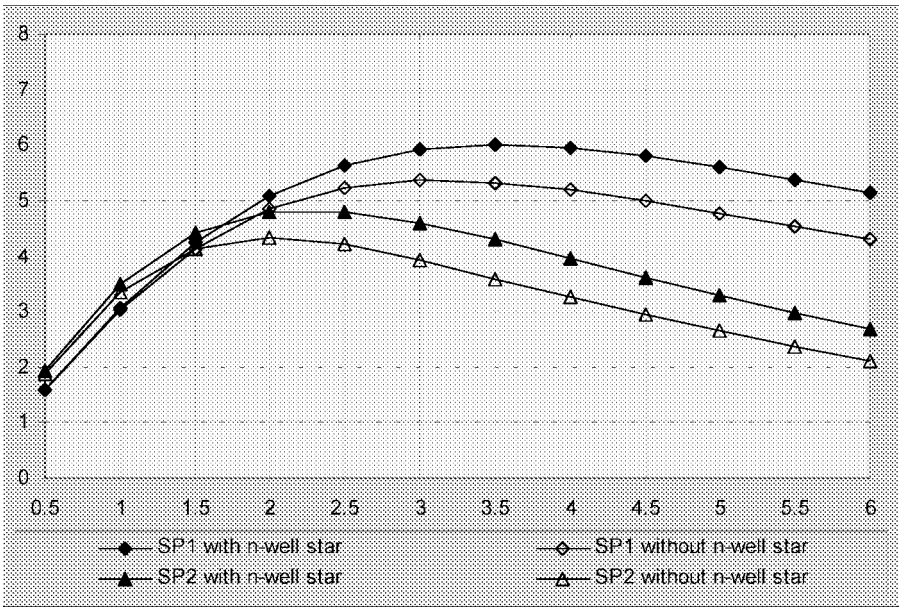

Fig. 3. Quality factor versus frequency at the measured inductors (see Table I for spiral details).

TABLE I
SPIRAL PARAMETERS

Spirals	SP1nw	SP1	SP2nw	SP2
number of turns	2	2	3	3
width of lines [um]	24	24	24	24
Nwell struct.	Yes	No	Yes	No
Ls [nH]	1.81	1.80	2.82	2.81
Cf [fF]	23	14	49	51
Cs1 [fF]	437	415	580	556
Cs2 [fF]	334	383	428	458
Rs1 [Ohm]	308	291	354	338
Rs2 [Ohm]	522	399	429	335
f(Qmax)[GHz]	3.5	3.5	2.0	2.0
Qmax	6.0	5.3	4.8	4.3
Ro [Ohm]	3.5	3.5	4.5	4.6
Leff @ 2GHz	1.82	1.82	2.90	2.90
Reff @ 2GHz	4.5	4.7	7.4	7.8

measurements on the spirals up to 6 GHz. By circuit optimization we extracted the parameters of the compact equivalent circuit (see Fig. 2). In Table I, the parameters of the spirals are summarized. Fig. 3 shows the quality factor of the spirals versus frequency, where we can see the improvement caused by the eddy-current blocking structure. We observed an increase from 5.3 to 6.0 at 3.5 GHz at an 1.8-nH inductor and from 4.3 to 4.8 at 2.2 GHz at an 2.8-nH inductor.

IV. CONCLUSIONS

A new method was introduced to improve the quality factor of the integrated spiral inductors at silicon RF IC's. The loss reduction is based on blocking the eddy currents in the semiconductive top p+ substrate layer with n+ stripes placed perpendicular to the eddy-current flow. The method was proved by measurements. With the described improvement our fully integrated voltage-controlled oscillator's (VCO's) phase noise performance became comparable with the ones having off-chip PCB resonators.

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